WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Saturday, March 20, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
□	L36	5740415.uref.	4
		DB=USPT,PGPB; PLUR=NO; OP=ADJ	
□	L35	branch$3 same L34	0
□	L34	"same block address"	84
□	L33	(L30 or L31) same branch$3	4
□	L32	"same bundle address"	0
□	L31	"same cache line address"	27
□	L30	"same line address"	67
□	L29	5805878.uref.	16
□	L28	L25 same Simultaneous$2	31
□	L27	L25 same L26	0
□	L26	"same address"	12363
□	L25	(multiple branch$2) with predict$3	121
		DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ	
□	L24	branch$3 and L23	16
□	L23	fetch$3 with correct$3 with address$3	98
□	L22	fetch$3 with correct$3 with L6	0
□	L21	correct$3 with bundle with address$3	4
□	L20	branch$3 and L19	0
□	L19	correct$3 with line with address$3	480
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
□	L18	l17 and (L10 or l2)	33
□	L17	correct$3 with line with address$3	1809
□	L16	l14 and (L10 or l2)	3
□	L15	l10 and (L14 or l2)	48
□	L14	correct$3 with bundle with address$3	14
□	L13	l10 and L12	3
□	L12	correct$3 with l6	388
□	L11	l6 and L10	57
□	L10	712/237,238,239,240.ccls.	686
□	L9	bundle address$3 and l2	0

□	L8	l2 and l6	19
□	L7	fetch$3 with correct$3 with L6	2
□	L6	block address$3	7574
□	L5	l2 and L4	17
□	L4	correct$3 with fetch$3 with (index$3 or address$3)	537
□	L3	l1 and L2	3
□	L2	712/234.ccls.	306
□	L1	712/206.ccls.	166

END OF SEARCH HISTORY

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□	L35	branch$3 same L34	0
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□	L18	l17 and (L10 or l2)	33
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□	L16	l14 and (L10 or l2)	3
□	L15	l10 and (L14 or l2)	48
□	L14	correct$3 with bundle with address$3	14
□	L13	l10 and L12	3
□	L12	correct$3 with l6	388
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□	L6	block address$3	7574
□	L5	l2 and L4	17
□	L4	correct$3 with fetch$3 with (index$3 or address$3)	537
□	L3	l1 and L2	3
□	L2	712/234.ccls.	306
□	L1	712/206.ccls.	166

END OF SEARCH HISTORY

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□ Generate Collection Print

L5: Entry 14 of 17 File: USPT Apr 14, 1998

US-PAT-NO: 5740415
DOCUMENT-IDENTIFIER: US 5740415 A

TITLE: Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy

DATE-ISSUED: April 14, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hara; Tetsuya	Hyogo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 08/ 538494 [PALM]
DATE FILED: October 3, 1995

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	6-246346	October 12, 1994

INT-CL: [06] G06 F 9/00, G06 F 9/32

US-CL-ISSUED: 395/585; 395/581, 395/580
US-CL-CURRENT: 712/238; 712/233, 712/234

FIELD-OF-SEARCH: 395/585, 395/581, 395/580

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
□	5530825	June 1996	Black et al.	395/421.03
□	5584001	December 1996	Hoyt et al.	395/585
□	5628021	May 1997	Iadonato et al.	395/800

OTHER PUBLICATIONS

"Branch Prediction Strategies and Branch Target... ", J.K. F. Lee et al., IEEE, Computer vol. 15, No. 1, Jan. 1984, pp. 6-22, cited on page four of the specification.
"Computer Architecture: Quantative Approach", D. A. Patterson, Morgan-Kaufman Publishers, published 1990, pp. 307-314.

ART-UNIT: 235

PRIMARY-EXAMINER: Lim; Krisna

ATTY-AGENT-FIRM: Lowe, Price, LeBlanc & Becker

ABSTRACT:

A branch execution unit processes operand data which is supplied from an instruction decoder with branch instruction information which is read from a branch target buffer, carries out branch prediction and execution, and forms a branch probability flag which is generated in relation to a branch instruction for supplying to a branch target buffer registration/update decision mechanism. In registration of a branch instruction which is non-registered in the BTB registration/update decision mechanism, the registration or non-registration is carried out in accordance with the value of the branch probability flag. Thus, it is possible to prevent a branch instruction having a low branch probability from being registered in the branch target buffer, thereby preventing reduction of branch prediction accuracy. The branch prediction is executed with employment of only a validity bit. Thus provided is an instruction processing apparatus including a branch target buffer which can be readily constructed with high branch prediction accuracy and causes no cycle penalty upon registration of a branch instruction or updating of the content thereof.

27 Claims, 51 Drawing figures

First Hit Fwd Refs

□ Generate Collection Print

L5: Entry 14 of 17 File: USPT Apr 14, 1998

DOCUMENT-IDENTIFIER: US 5740415 A
TITLE: Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy

Brief Summary Text (18):
If a determination is made that the decided branch condition mismatches with the prediction at the step S7, i.e., when the prediction is erroneous, on the other hand, the fetched branch target instruction is invalidated and instruction fetching is carried out in accordance with a correct address, while the corresponding entry 1a of the branch target buffer 1 is updated (this branch target buffer updating operation is also described later) (step S9).

Current US Cross Reference Classification (2):
712/234

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L16: Entry 1 of 3   File: USPT   Oct 12, 1999

US-PAT-NO: 5964869
DOCUMENT-IDENTIFIER: US 5964869 A

TITLE: Instruction fetch mechanism with simultaneous prediction of control-flow instructions

DATE-ISSUED: October 12, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Talcott; Adam R.	Santa Clara	CA		
Panwar; Ramesh K.	Santa Clara	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Palo Alto	CA			02

APPL-NO: 08/ 878753 [PALM]
DATE FILED: June 19, 1997

INT-CL: [06] G06 F 9/38

US-CL-ISSUED: 712/236; 712/240
US-CL-CURRENT: 712/236; 712/240

FIELD-OF-SEARCH: 395/583, 395/587, 395/585, 395/586, 712/236, 712/238, 712/239, 712/240

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

[Search Selected] [Search ALL] [Clear]

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4777587	October 1988	Case et al.	395/582
☐	5101341	March 1992	Circello et al.	
☐	5142634	August 1992	Fite et al.	
☐	5283873	February 1994	Steely, Jr. et al.	
☐	5394529	February 1995	Brown, III et al.	395/587
☐	5394530	February 1995	Kitta	395/587
	5440717	August 1995	Bosshart	

□				
□	5454117	September 1995	Puziol et al.	
□	5461722	October 1995	Goto	395/582
□	5553255	September 1996	Jain et al.	
□	5592634	January 1997	Circello et al.	395/586
□	5604909	February 1997	Joshi et al.	395/384
□	5613081	March 1997	Black et al.	711/3
□	5623614	April 1997	Van Dyke et al.	
□	5708788	January 1998	Katsuno et al.	
□	5732253	March 1998	McMahan	

OTHER PUBLICATIONS

Yeh. et al., "Branch History Table Indexing to Prevent Pipeline Bubbles in Wide-Issue Supersealar Processors",Proceedings of the 26th Annual International Symposium on Microarchitecture, 1993, pp. 164-175, IEEE, Dec. 1-3, 1993.
Yeh, et al, "A Comprehensive Instruction Fetch Mechanism for a Processor Supporting Speculative Execution," Department of Electrical Engineering and Computer Science, University of Michigan, IEEE Publication 1992, pp. 129-139.

ART-UNIT: 274

PRIMARY-EXAMINER: Treat; Wiiliam M.

ATTY-AGENT-FIRM: Conley, Rose & Tayon, PC Kivlin; B. Noel

ABSTRACT:

A microprocessor is provided with an instruction fetch mechanism that simultaneously predicts multiple control-flow instructions. The instruction fetch unit further is capable of handling multiple types of control-flow instructions. The instruction fetch unit uses predecode data and branch prediction data to select the next instruction fetch bundle address. If a branch misprediction is detected, a corrected branch target address is selected as the next fetch bundle address. If no branch misprediction occurs and the current fetch bundle includes a taken control-flow instruction, then the next fetch bundle address is selected based on the type of control-flow instruction detected. If the first taken control-flow instruction is a return instruction, a return address from the return address stack is selected as the next fetch bundle address. If the first taken control-flow instruction is an unconditional branch or predicted taken conditional branch, a predicted branch target address is selected as the next fetch bundle address. If no branch misprediction is detected and the current fetch bundle does not include a taking control-flow instruction, then a sequential address is selected as the next fetch bundle address.

18 Claims, 5 Drawing figures

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L16: Entry 1 of 3 File: USPT Oct 12, 1999

DOCUMENT-IDENTIFIER: US 5964869 A
TITLE: Instruction fetch mechanism with simultaneous prediction of control-flow instructions

Abstract Text (1):

A microprocessor is provided with an instruction fetch mechanism that simultaneously predicts multiple control-flow instructions. The instruction fetch unit further is capable of handling multiple types of control-flow instructions. The instruction fetch unit uses predecode data and branch prediction data to select the next instruction fetch bundle address. If a branch misprediction is detected, a corrected branch target address is selected as the next fetch bundle address. If no branch misprediction occurs and the current fetch bundle includes a taken control-flow instruction, then the next fetch bundle address is selected based on the type of control-flow instruction detected. If the first taken control-flow instruction is a return instruction, a return address from the return address stack is selected as the next fetch bundle address. If the first taken control-flow instruction is an unconditional branch or predicted taken conditional branch, a predicted branch target address is selected as the next fetch bundle address. If no branch misprediction is detected and the current fetch bundle does not include a taking control-flow instruction, then a sequential address is selected as the next fetch bundle address.

Brief Summary Text (13):

The problems outlined above are in large part solved by a microprocessor in accordance with the present invention. In one embodiment, a microprocessor includes an instruction fetch unit with simultaneous prediction of multiple control-flow instructions. The instruction fetch unit fetches a group of N instructions, called the current fetch bundle, each instruction fetch cycle. For the purposes of this disclosure, an "instruction fetch cycle" refers to a clock cycle or cycles in which instructions are fetched from cache or memory for dispatch into the instruction processing pipeline. The current fetch bundle includes the instruction located at a current fetch bundle address and the N-1 subsequent instructions in sequential order. For each current fetch bundle, the instruction fetch unit generates one or more predicted branch target addresses, a sequential address, a return address, and, if a misprediction is detected, a corrected branch target address. Based upon the detection of a branch misprediction and/or the occurrence of control-flow instructions within the current fetch bundle, branch logic selects one of the above addresses as the next fetch bundle address.

Brief Summary Text (14):

If a branch misprediction is detected, the corrected branch target address is selected as the next fetch bundle address. If no branch misprediction is detected, the control-flow instructions with the current fetch bundle are identified. If the first "taken" control-flow instruction is a return from a call instruction, the return address is selected as the next fetch bundle address. For the purposes of the disclosure, a "taken control-flow instruction" may be an unconditional control-flow instruction, such as a unconditional branch or return instruction, or a conditional branch instruction that is predicted "taken". If the first control-flow instruction is an unconditional branch, one of the predicted branch target addresses is selected as the next fetch bundle address. If the first control-flow instruction is a conditional branch instruction that is predicted taken, one of the predicted branch addresses is selected as the next fetch bundle address. If no "taken control-flow instructions" are within a fetch bundle, the sequential address is selected as the next fetch bundle address. The sequential address is the address of the fetch bundle that is numerically sequential to the current fetch bundle. If a fetch bundle includes eight instructions, the sequential address is the current fetch bundle address plus the number of addresses occupied by the eight instructions. For example, if instructions are byte addressable and each instruction is thirty-two bits, the sequential address is the current fetch bundle address plus thirty-two.

Brief Summary Text (16):
Generally speaking, the present invention contemplates an instruction fetch unit that concurrently makes multiple predictions for different types of control-flow instructions including a branch address table, a sequential address circuit, an unresolved branch circuit, a multiplexer and a branch logic circuit. The branch address table is configured to store predicted branch target addresses for branch instructions and to output a predicted branch target address signal. The sequential address circuit is configured to calculate a sequential address and to output a sequential fetch address signal. The unresolved branch circuit is configured to store a corrected branch target address for a mispredicted branch instruction and to output a corrected branch target address signal. The multiplexer is coupled to receive a plurality of input signals including the predicted branch target address signal, the sequential fetch address signal and the corrected branch target address signal, and configured to output a current fetch bundle address signal that addresses a fetch bundle. The branch logic circuit is coupled to a control signal of the multiplexer. The branch logic circuit is configured to cause the multiplexer to select one of the plurality of input signals in dependence on an occurrence of a control-flow instruction within the fetch bundle or an occurrence of a mispredicted branch instruction.

Brief Summary Text (17):
The present invention further contemplates a method for concurrently making multiple predictions of different types of control-flow instructions including: generating a sequential fetch address, wherein the sequential fetch address is an address of a fetch bundle sequential in numerical order to a current fetch bundle; generating a predicted branch target address; generating a corrected branch target address, wherein the corrected branch target address is the correct target address of mispredicted branch instruction; detecting a branch misprediction, wherein if a branch misprediction is detected, the corrected branch target address is selected as a next fetch bundle address; and detecting a first taken control-flow instruction. If the first taken control-flow instruction is an unconditional branch instruction, the predicted branch target address is selected as the next fetch bundle address. If the first taken control-flow instruction is a taken conditional branch instruction, the predicted branch target address is selected as the next fetch bundle address. If neither a branch misprediction or a taken control-flow instruction is detected, the sequential fetch address is selected as the next fetch bundle address. A next fetch bundle is retrieved using the next fetch bundle address.

Detailed Description Text (42):
In step 509, the occurrence control-flow instructions are detected using predecode data, and branch prediction data is used to predict whether any control-flow instructions are predicted taken or not taken. In one embodiment, a taken control-flow instruction is defined as an unconditional control-flow instruction such as a return instruction or a conditional control-flow instruction, such as a branch-on-zero instruction, that is predicted taken. In one embodiment, steps 510, 514, 518, 524 and 528 are performed in parallel. In step 510, it is determined whether a branch misprediction occurred in an instruction execution cycle. In one embodiment, a branch misprediction occurs when either a branch is mispredicted as taken or not

taken or a branch target address is mispredicted. If a branch misprediction is detected in step 510, then in step 512 the corrected branch target address generated in step 508 is selected as the next fetch bundle address. In step 514 it is determined whether any taken control-flow instructions are included in the fetch bundle. If no taken control-flow instructions are detected in the fetch bundle, then in step 516 the sequential address generated in step 504 is selected as the next fetch bundle address. In step 518, it is determined whether the first taken control-flow instruction is a return instruction. If in step 518, it is determined the first taken control-flow instruction is a return instruction, then in step 520 a return address is selected as the next fetch bundle address. In one embodiment, the return address is stored on a return address stack. Return addresses are pushed on the stack as call instructions are executed. In step 524, it is determined whether the first control-flow instruction is an unconditional branch instruction. If the first control-flow instruction is an unconditional branch, then in step 526 the predicted branch target address generated in step 506 is selected as the next fetch bundle address. In step 528 it is determined whether the first taken control-flow instruction is a conditional branch instruction that is predicted taken. If the first control-flow instruction is a taken conditional branch instruction, then in step 526 the predicted branch target address generated in step 506 is selected as the next fetch bundle address.

Current US Cross Reference Classification (1):
712/240

CLAIMS:

1. An instruction fetch unit that concurrently makes multiple predictions for different types of control-flow instructions comprising:

a branch address table configured to store predicted branch target addresses for branch instructions and to output a predicted branch target address signal;

a sequential address circuit configured to calculate a sequential address and to output a sequential fetch address signal;

an unresolved branch circuit configured to store a corrected branch target address for a mispredicted branch instruction and to output a corrected branch target address signal;

a multiplexer coupled to receive a plurality of input signals including said predicted branch target address signal, said sequential fetch address signal and said corrected branch target address signal, and configured to output a current fetch bundle address signal that addresses a fetch bundle;

a branch logic circuit coupled to provide a control signal to said multiplexer, wherein said branch logic circuit is configured to cause said multiplexer to select one of said plurality of input signals in dependence on an occurrence of a control-flow instruction within said fetch bundle or an occurrence of a mispredicted branch instruction; and

a predecode circuit configured to generate an array of predecode bits that identifies a type of instructions within said fetch bundle, wherein said branch logic circuit is configured to use said array of predecode bits to identify an occurrence and location of control-flow instructions.

10. An instruction fetch unit that concurrently makes multiple predictions for different types of branches comprising:

a branch address table configured to store predicted branch target addresses for branch instructions and to output a predicted branch target address signal;

a sequential address circuit configured to calculate a sequential address and to output a sequential fetch address signal;

a return address unit configured to store a return address for a call instruction and configured to output a return address signal;

a branch misprediction recovery circuit configured to store a corrected branch target address for a mispredicted branch instruction and to output a corrected branch target address signal;

a multiplexer coupled to receive a plurality of input signals including said predicted branch target address signal, said sequential fetch address signal, said return address signal and said corrected branch target address signal, and configured to output a fetch bundle address signal that addresses a fetch bundle;

a branch predictor coupled to said fetch bundle address signal and said branch logic circuit, wherein said branch predictor predicts whether conditional branches within said fetch bundle are taken or not taken

a branch logic circuit coupled to a control signal of said multiplexer, wherein said branch logic circuit is configured to cause said multiplexer to select one of said plurality of input signals in dependence on the occurrence of a control-flow instruction within said fetch bundle or the occurrence of a mispredicted branch instruction;

a predecode circuit configured to generate an array of predecode bits that identifies a type of instructions with said fetch bundle, wherein said branch logic circuit is configured to use said array of predecode bits to identify the occurrence and location of branch instructions.

11. An instruction fetch unit that concurrently makes multiple predictions for different types of control-flow instructions comprising:

a branch address table configured to store predicted branch target addresses for branch instructions and to output two predicted branch target address signals;

a sequential address circuit configured to calculate a sequential address and to output a sequential fetch address signal;

an unresolved branch circuit configured to store a corrected branch target address for a mispredicted branch instruction and to output a corrected branch target address signal;

a multiplexer coupled to receive a plurality of input signals including said predicted branch target address signal, said sequential fetch address signal and said corrected branch target address signal, and configured to output a current fetch bundle address signal that addresses a fetch bundle; and

a branch logic circuit coupled to provide a control signal to said multiplexer, wherein said branch logic circuit is configured to cause said multiplexer to select one of said plurality of input signals in dependence on an occurrence of a control-flow instruction within said fetch bundle or an occurrence of a mispredicted branch instruction;

wherein said branch address table is configured to output said two predicted branch target address signals to said multiplexer for each fetch bundle, and said branch logic circuit is configured to cause said multiplexer to select one of said two predicted branch target address signals in dependence on a location of a first unconditional branch instruction or a first taken conditional branch instruction within said fetch bundle.